Impact of CMOS Scaling on Single-Event Hard Errors in Space Systems

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Abstract

Applications of highly scaled devices in space applications are shown to be limited by hard errors from cosmic rays. Hard errors were first observed in 0.8 μm DRAMs. For feature sizes below 0.5 μm, scaling theory predicts that low power devicees will have much lower hard error rates than devices optimized for high speed.

introduction

Recent emphasis on low-power electronics for laptop computers, along with fundamental limitations in maintaining hot-carrier reliability, have resulted in new commercial devices with reduced supply voltage, and future devices with power supply voltages in the 1 .5-2 V range are predicted by the year 2000. [1,2] Low-power technologies are extremely attractive for future spacecraft which are heavily constrained to reduce power, weight, and cost. This paper discusses the effect of scaling on the sensitivity of VLSI devices to hard errors from cosmic rays, which have recently been observed in commercial DRAMs. The hard-error problem was first observed for devices with feature sizes of 0.8 μm, and it is likely to become the dominant factor in applying highly scaled devices in space. [3,4]

Conventional and Low-Power Device Scaling

Older device scaling approaches have generally followed two assumptions: constant-field scaling, which allows the power supply voltage to be scaled along with other parameters to optimize device structure; and constant-voltage scaling, 'which has fixed the supply voltage in order to assure compatibility with applications. [5,6] More recent studies have recognized that a new sealing approach is needed below 0.5 μm to overcome the loss of drive and limited ability to reduce threshold voltage (V_t), which require aggressive scaling of gate oxide thickness and electric field. [7-l 0]

Predictions of oxide field strength for smaller feature sizes are shown in Figure 1 for two scaling approaches, one optimized for speed and circuit performance, and the other for low power. The speed-optimized scaling curve predicts a rapid rise in gate oxide field as feature sizes are reduced below 0.5 pm, but the scaling curve that is optimized for low-power devices exhibits a plateau below 0.25 μm. As discussed in the next section, oxide fields above 3.5 MV/cm are likely to increase hard-error rates to unacceptable levels in space applications because the sensitivity of devices to catastrophic errors is strongly affected by the electric field in the gate oxide.

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Hard Error Results and Scaling Predictions

During the last two years, two types of hard errors have been observed in DRAMs during laboratory testing at high energy accelerators which are used to simulate the effects of comic rays on electronic devices intended for space use. Hard errors are the result of the interaction of a single heavy ion with a small-area device, causing permanent failure. They are statistically unlikely, but occur for a small number of transistors on a VLSI device when it is exposed to heavy ions. As device geometries are reduced, the probability of occurrence increases,

The first mechanism is due to microscopic ionization damage from the passage of a single ion (or a small number of ions) within the gate. [3] The hole traps that result change V_t, increasing subthreshold leakage of the particular transistor that was struck by the ion. This effect is primarily important for DRAMs or 4-T SRAMS that use dynamic storage, but is not expected to be significant for random logic or 6-T SRAMs.

The second mechanism causes catastrophic shorting of the gate oxide in the specific transistor that is struck by the heavy ion, [4] It is attributed to gate rupture, and occurs because the high charge density produced by the ion track alters the electric field under the gate, increasing the gate voltage. If the gate is initially biased prior to the ion strike, the additional electric field produced by the transient can increase to a sufficiently high value to cause gate oxide breakdown. Although such effects have been studied for several years in power MOSFETs, they have only recently been observed for VLSI devices. Gate rupture can occur for random logic as well as memories, and will likely prevent the use of extremely scaled devices in space. J}'L. has studied gate. rupture in a commercial 4-Mb DRAM. Two versions of this device were tested; the second version was redesigned to reduce the dimensions by 20%, and had a thinner gate oxide. 130th versions operated with five-volt power supplies. Hard errors were observed for the initial version of the device when it was irradiated with heavy ions that produced a linear charge density of 0.8 pC/μm, but not for heavy ions with lower charge densities, The hard-error threshold for the shrunk device was 0.6 pC/μm. These results are summarized in Figure 2. The dashed line shows a prediction of the effect of future scaling changes, assuming that the threshold for gate rupture scales as $(E_{ox})^{-2}$, osing oxide fields from high-speed scaling. For low-power scaling, the threshold charge generation limit decreases much more slowly.

In order to interpret these results, one must take into account the distribution of galactic cosmic rays, which decrease rapidly for high linear charge densities. Above 0.3 pC/μm, the distribution falls abruptly by more than three orders of magnitude. These results have been used to calculate the catastrophic

hard-error rate for devices with different feature sizes, as shown in Figure 3. The error rate in the figure represents the number of failed devices for a VLSI circuit with one-million transistors. There is a pronounced difference in the error rate for the two different scaling approaches. The very rapid increase in the error rate of the high-speed scaling curve occurs when the threshold charge density falls below 0.3 pC/μm, where there is a large jump in the number of cosmic-ray particles. The curve suggests that it will be very difficult to use devices with 0.25 μm feature size because of the hard-error limit, and that devices optimized for low-power operation will have a much lower error rate in space applications.

Discussion and Summary

Hard errors from cosmic rays are an important new effect that will ultimately limit the circuit technologies used for space applications. Although hard errors have been initially observed in memories, it is possible to overcome memory errors using basic error-detection-and-correction techniques. Hard errors in other types of circuits, such as microprocessors or random logic, are potentially far more serious, and may cause catastrophic failure of space hardware unless new architectures are employed that can deal with hard errors in internal logic circuits.

The hard-error problem is a direct result of device scaling, which has pushed electric fields to much higher values, and reduced device dimensions to the point that device size is comparable to the size of microscopic damage regions from heavy ions. It has not been important in existing space systems, which have generally used much older technologies. The results of this paper show that hard errors begin to be significant for feature sizes below 0.5 μm, and that very high error rates are expected for highly scaled technologies in the future.

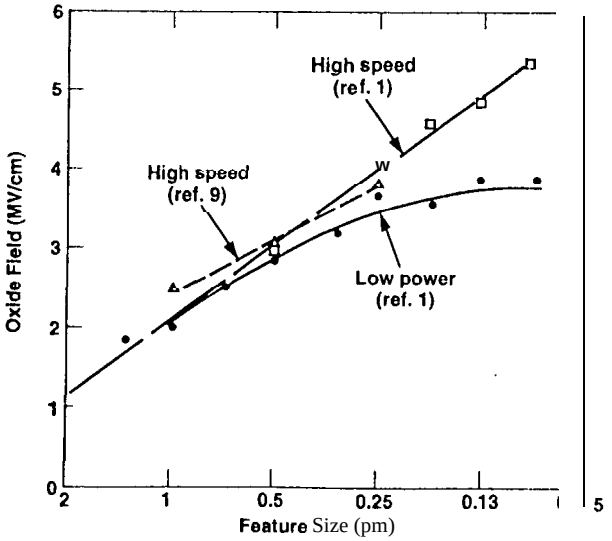

Figure 1. Effect of device scaling on gate oxide field. (Note [he inverted scale on the abscissa)

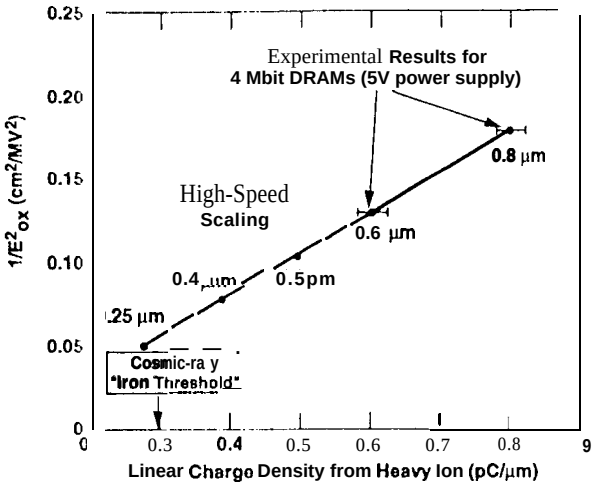

Figure 2. Effect of device scaling on hard-error threshold for various feature sizes.

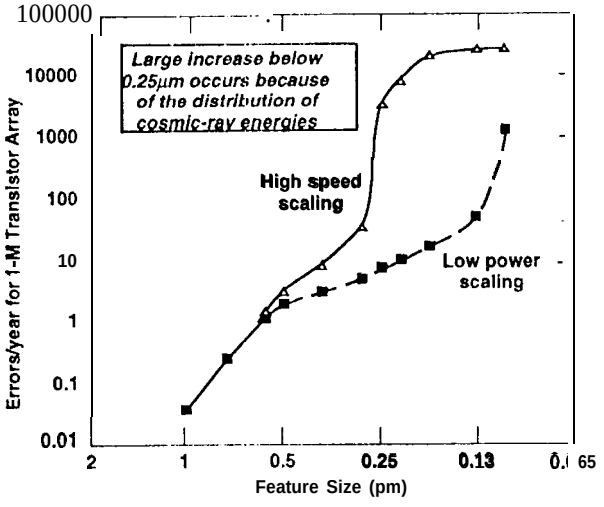

Figure 3. Hard errors induced by cosmic rays for a 1-M transistor array as feature sizes are reduced (geosychronous space orbit).

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